ENGINNEERING SIO2/TIO2 STACKS FOR IMPROVED ELECTRON SELECTIVE CONTACTS

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ABSTRACT: To increase the conversion efficiency of crystalline silicon solar cells, reduction of the recombination losses associated with the contacts is a must. Therefore, a contact structure that simultaneously passivates the c-Si surface while selectively extracting only one type of charge carrier (i.e., either electrons or holes) is desired. Therefore, recently such passivating contacts in c-Si solar cells has become an important research objective.
Oxide/poly-Si concepts have been used to successfully reduce contact recombination. However, the use of poly-Si, namely at the front contact, introduces unwanted absorption of the sunlight. So, in addition to the electrical properties, the optical losses have to be minimized both on the front and rear sides of the solar cell for any contact structure. Furthermore, we aim at developing high quality selective contacts that can be deposited easily and economically. To address the problem caused by absorption in the top contact we studied different stacks using SiO2 and Ti and TiO2 layers with variable combinations, along two routes: high temperature route, in which the silicon oxide is obtained by thermal oxidation and a low temperature route where the silicon oxide is obtained by chemical oxidation or by e-beam evaporation.
The results show that the introduction of the additional Ti layer is not beneficial when compared to stacks without this layer. High temperature thermal SiO2 (900C) gives lower lifetimes when compared to the low temperature thermal oxide (775C). Annealing is crucial to enhance the final lifetimes in all explored stacks.
Keywords: Selective Contacts, SiO_2, TiO_2

1 INTRODUCTION

Several improvements have been introduced to enhance solar cell efficiency, being it by improving cell structure such as textured surfaces for light trapping structures, antireflective coatings, or by improving material quality such as high-quality Si wafers (N-type FZ-Si, N-type CZ-Si) used to reduce bulk recombination. The work present here incorporates innovative carrier selective junctions (CSJs). These CSJs overcome the major limitation of today's solar cells – recombination losses - while efficiently extract the electrical current generated in the solar cell [1]. CSJs can therefore be considered as a major asset for the achievement of ultra-high efficiencies. We explore the effect of introducing a 1 nm Ti layer in the TiO2-SiO2 interface with the intent to affect the stoichiometric relation between Ti-O in the transition region.

2 EXPERIMENTAL PROCEDURE

2.1 Experimental approach

In order to be able to test the contact tunneling ability of the SiO_2 layers, and passivating ability of the stacks of SiO2+TiO2 [2][3] and SiO2+Ti+TiO2, a sandwich like structure (figure 1) was produced in order to achieve equivalent passivation and conductivity in both sides of the samples.

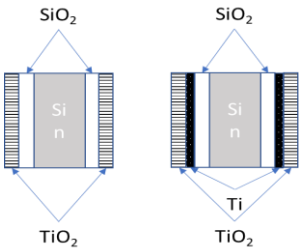

Figure 1: Representation of the general structure of both stack formats tested. On the left: TiO_2 deposited over SiO_2; on the right: TiO_2 on top of Ti on top of SiO_2.

At each step of the stack preparation. minority carrier lifetime measurements were taken.
Both these structures were tested under two routes for the SiO_2 layer formation: a high temperature route and a low temperature route. The general procedure for the sample preparation in represented in figure 2.

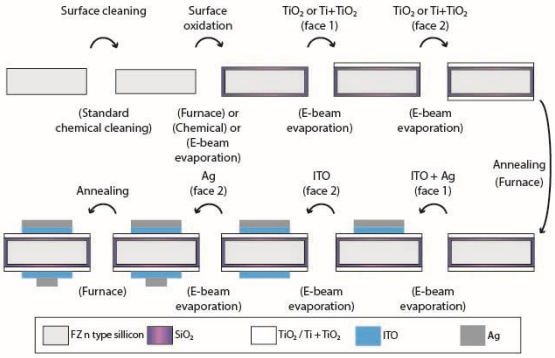

Figure 2: Sample preparation procedure sequence.

2.2. Oxidation

All samples where formed out of FZ n-type silicon, with 1-5 Ohm.cm resistivity, 125 cm round wafers, cleaved in 9 pieces. Prior to the oxidation process, all samples where cleaned with standard cleaning solutions of $HCl+H_2O_2+H_2O$ and $NH_4OH+H_2O_2+H_2O$ for 10 minutes at 85ºC, each of them followed by a dip in a diluted HF and rinsed in deionized water.
For the formation of the SiO_2 layer, three methods where used, defining a high temperature route, with thermal dry oxidation and a low temperature route, with e-beam evaporation of SiO_2 and chemical oxidation.
For the thermal oxidation, tubular furnaces where used with O_2 enriched atmosphere and two sets where produced at 900ºC and at 775ºC, both for 90 minutes.
The chemical oxidation was achieved by immersing the samples in concentrated HNO_3 at 90ºC, for 30 minutes, rinsed afterward in DI water.

For the SiO_2 layer applied by e-beam evaporation, the process had to be replicated for each side of the sample and was done in sequence with the deposition of TiO_2 or $Ti+TiO_2$ for each side.

2.3 TiO_2/ $Ti+TiO_2$

The TiO_2 layer was applied to the samples by e-beam evaporation in two evaporation runs, one for each sample side, and similarly happened with the $Ti+TiO_2$ stack. The thicknesses applied were of 1 nm of titanium and 10 nm of titanium oxide for all samples, and the thickness was controlled by a crystal oscillator thickness measuring system.

All samples were annealed in forming gas for 5 minutes at 350ºC, after de TiO_2 layer evaporation.

2.4 ITO and Ag layers

A further layer of ITO (indium tin oxide) was evaporated on each side of each sample in two concentric disks with 20 mm diameter, topped with a silver layer also e-beam evaporated. This was intended to enable measuring the current-voltage response of the stacks under test. After this step, the samples were subjected to a new annealing, with the same previously described characteristics.

3 RESULTS

3.1. SiO_2 thickness

The thickness of the SiO_2 was measured by ellipsometry for the thermal and chemical oxidation and the e-beam evaporation thickness was measured by the thickness control crystal oscillator system embedded in the evaporation equipment. The results are summarized in the table I

Table I: SiO2 layer thickness obtained by the different methods

	SiO_2 thickness (nm)
Thermal oxidation at 900ºC	20
Thermal oxidation at 775ºC	3
Chemical oxidation	1
E-Beam evaporation	10

3.2. Lifetime

We focused on the evolution of the minority carrier lifetime along the contact formation. Lifetime measurements were taken in three moments with Sinton WTC-120: 1) after SiO_2 layer formation, 2) after TiO_2 layer evaporation and 3) after annealing. Both paths of the low temperature SiO_2 route, chemical oxidation (figure 3) and SiO_2 evaporation (figure 4), presented similar evolutions, revealing an increase in effective lifetime, after annealing, and no visible difference before and after TiO_2 deposition evaporation. In this scope, it is yet observed an increased lifetime level with evaporated SiO_2 (figure 4) against SiO_2 achieved by chemical oxidation (figure 3).

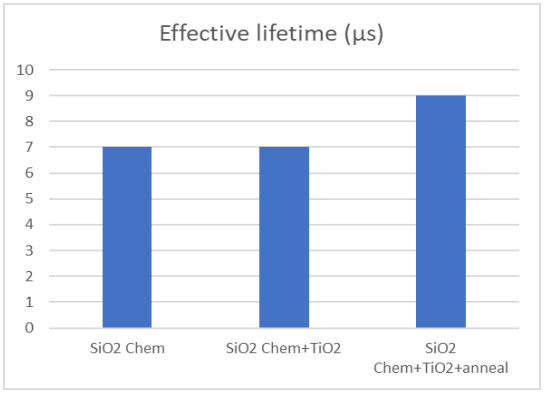

Figure 3: Effective minority carrier lifetime evolution across the stack formation with chemically grown SiO_2.

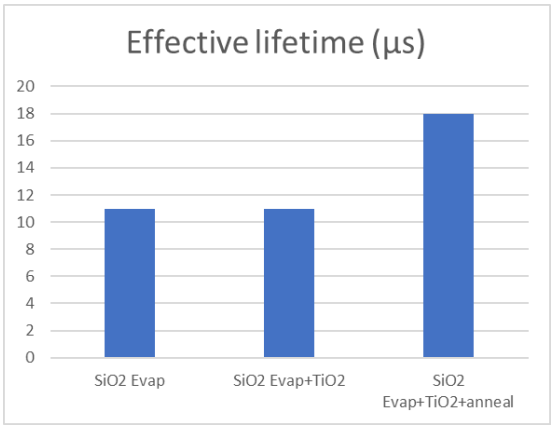

Figure 4: Effective minority carrier lifetime evolution across the stack formation with SiO_2 deposited by e-beam evaporation.

On the high temperature route to SiO_2, two different temperatures were tested for the thermal oxidation, and the observed evolutions of effective lifetime along the stack construction opposite results. The lower temperature (775ºC) oxidation, (figure 5), resulted in an effective lifetime comparable with the evaporated SiO_2, (figure 4), however a very significant increase in effective lifetime was achieved after annealing. At the higher temperature oxidation (900ºC) (figure 6), a reversed behavior was observed, with higher lifetime immediately after oxidation, suffering a significant drop after annealing, to a lower level than the annealed, 775ºC thermal oxide.

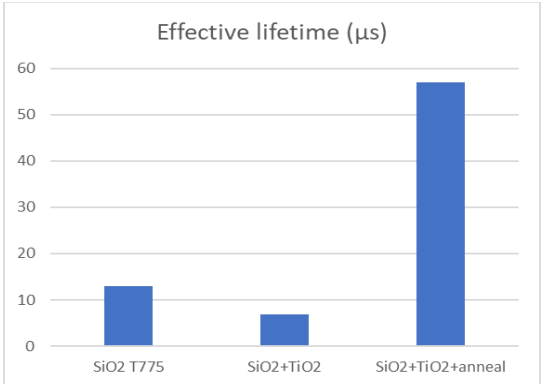

Figure 5: Effective minority carrier lifetime evolution across the stack formation with SiO_2 grown by thermal oxidation at 775ºC.

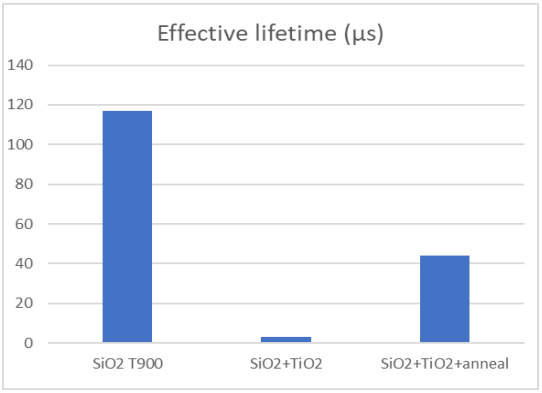

Figure 6: Effective minority carrier lifetime evolution across the stack formation with SiO_2 grown by thermal oxidation at 900ºC.

3.3 Ti layer impact

A systematic degradation of effective lifetime even after annealing, in all stacks containing the 1 nm Ti interlayer was observed. This degradation is most noted in the high temperature oxides highlighted in figure 7 and figure 8. Annealing is still important to recover effective lifetime measurement.

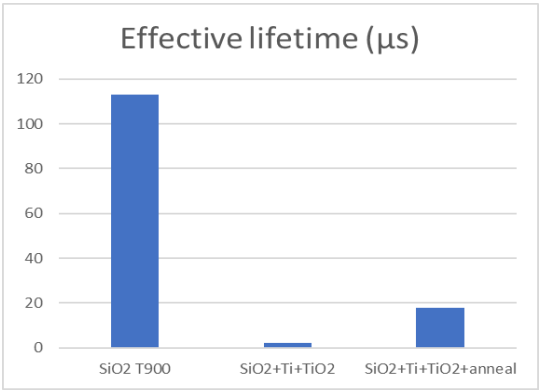

Figure 7: Effective minority carrier lifetime evolution across the stack formation, by introducing a 1 nm Ti layer in the SiO2-TiO2 interface, with SiO_2 grown by thermal oxidation at 900ºC.

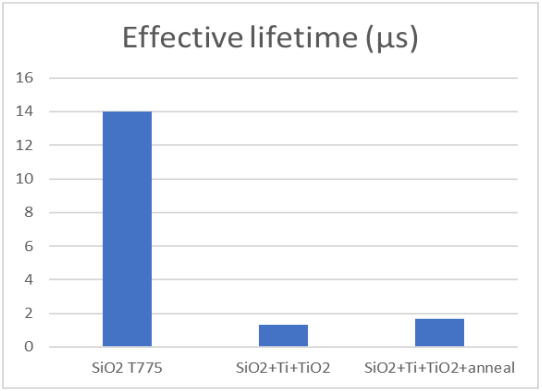

Figure 8: Effective minority carrier lifetime evolution across the stack formation, introducing a 1 nm Ti layer in the SiO2-TiO2 interface, with SiO_2 grown by thermal oxidation at 775ºC.

A positive impact of deploying the 1 nm Ti interlayer is visible in the current density measured across the stack. The low temperature thermal SiO_2 (775ºC) stack reveals a higher current density with the 1 nm Ti interlayer (figure 8). The high temperature thermal SiO_2 (900ºC) did not reveal a significant difference in the current density, with or without the Ti interlayer (figure 10), with its values at the level of low temperature thermal SiO_2 (775ºC) without Ti interlayer.

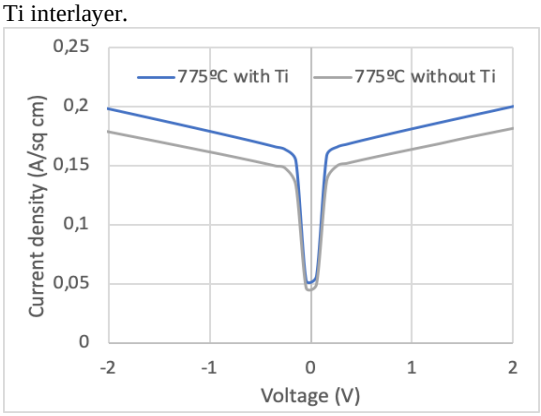

Figure 9: Plot of the current density across the stack versus voltage, for samples with thermally grown SiO_2 at 775ºC. Influence of the introduction of the 1 nm Ti layer in the SiO_2-TiO_2 interface (blue line) against the regular SiO_2-TiO_2 stack (grey line).

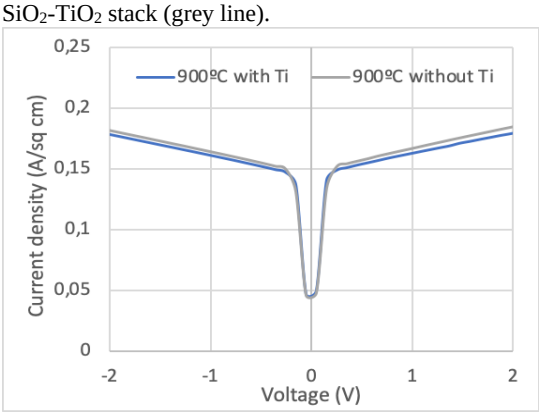

Figure 10: Plot of the current density across the stack versus voltage, for samples with thermally grown SiO_2 at 900ºC. Influence of the introduction of the 1 nm Ti layer in the SiO_2-TiO_2 interface (blue line) against the regular SiO_2-TiO_2 stack (grey line).

4 DISCUSSION

As expected, the silicon oxide layer obtained at higher temperature (900ºC) yielded by itself the best results for passivation prior to the addition of the TiO_2, layer. This SiO_2 layer was the thicker one and due to its process, better suited to achieve effective Si-SiO_2 bounds. As a passivating layer by itself, this 20nm SiO_2 layer, did not reveal to benefit in any way by the stacking up with neither TiO_2 nor Ti+TiO_2.

In all samples, a significant reduction of measured lifetime after the deposition of the Ti interlayer was observed. This may be due to the nature of the measurement technique which may be sensitive to metallic nature of the pre annealed Ti interlayer.

The low temperature thermal oxide stack revealed the highest, relative increase in effective minority carrier lifetime after annealing, expressing the formation of the selective carrier contact.

The 20nm SiO_2 layer thickness obtained by thermal oxidation, is excessive to effectively participate in the selective contact, as it is the only one to reveal a reduction

in lifetime after annealing the SiO_2-TiO_2 stack.

5 CONCLUSIONS

Low temperature thermal SiO_2 stack, show some benefit in current density from the 1 nm Ti layer, while the higher temperature SiO_2 samples do not present significant difference in current density, with both high temperature SiO_2 stack (with and without Ti) having comparable current densities to the low temperature SiO_2 sample without Ti layer.

We conclude that the option for lower temperature thermal oxidation (775ºC) provides better passivation, in addition to a better tunneling performance of the thinner oxide.

Annealing is crucial to enhance the final lifetimes and our best results shows effective lifetimes of 57 µs for the whole stack.

7 ACKNOWLEGEMNTS

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8 REFERENCES

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